MCP6G01/2/3/4

110 µA Selectable Gain Amplifier

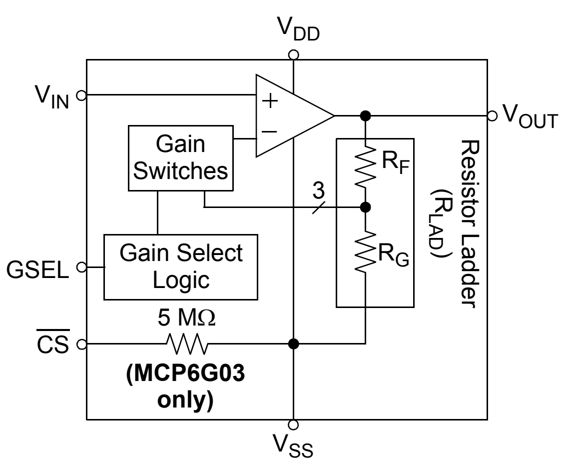
Features

- 3 Gain Selections:
  - +1, +10, +50 V/V
- One Gain Select Input per Amplifier
- Rail-to-Rail Input and Output
- Low Gain Error: ±1% (max.)
- High Bandwidth: 250 kHz to 900 kHz (typ.)
- Low Supply Current: 110 µA (typ.)
- Single Supply: 1.8V to 5.5V
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- A/D Converter Driver
- Industrial Instrumentation
- Bar Code Readers
- Metering
- Digital Cameras

Block Diagram



Gain (V/V)	GSEL Voltage (Typ.) (V)
1	V_{DD}/2 (or open)
10	0
50	V_{DD}

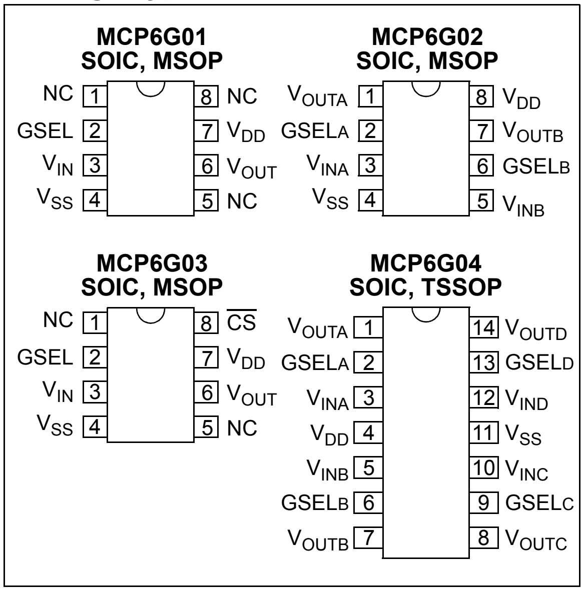
Note: V_{SS} is assumed to be 0V

Description

The Microchip Technology Inc. MCP6G01/2/3/4 are analog Selectable Gain Amplifiers (SGA). They can be configured for gains of +1 V/V, +10 V/V, and +50 V/V through the Gain Select input pin(s). The Chip Select pin on the MCP6G03 can put it into shutdown to conserve power. These SGAs are optimized for single supply applications requiring reasonable quiescent current and speed.

The single amplifier MCP6G01 and MCP6G03, and the dual amplifier MCP6G02, are available in 8-pin SOIC and MSOP packages. The quad amplifier MCP6G04 is available in 14-pin SOIC and TSSOP packages. All parts are fully specified from -40°C to +125°C.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Analog Input Pin (V_{IN}) ....±2 mA
Analog Input (V_{IN}) †† .... V_{SS} – 1.0V to V_{DD} + 1.0V
All other Inputs and Outputs........... V_{SS} – 0.3V to V_{DD} + 0.3V
Output Short Circuit Current..................continuous
Current at Output and Supply Pins .... ±30 mA
Storage Temperature....................-65°C to +150°C
Junction Temperature.............................+150°C
ESD protection on all pins (HBM; MM) .... ≥ 4 kV; 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.4 "Input Voltage and Current Limits"**.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier Inputs (V_{IN})						
Input Offset Voltage	V_{OS}	–4.5	±1.0	+4.5	mV	G = +1
		—	±1.0	—	mV	G = +10, +50
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	G = +1, T_A = -40°C to +125°C
Power Supply Rejection Ratio	PSRR	65	80	—	dB	G = +1 **(Note 1)**
Input Bias Current	I_B	—	1	—	pA	
Input Bias Current at	I_B	—	30	—	pA	T_A = +85°C
Temperature	I_B	—	1000	5000	pA	T_A = +125°C
Input Impedance	Z_{IN}	—	10^{13}‖6	—	Ω‖pF	
Amplifier Gain						
Nominal Gains	G	—	1 to 50	—	V/V	+1, +10 or +50
DC Gain Error G = +1	g_E	–0.3	—	+0.3	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
G ≥ +10	g_E	–1.0	—	+1.0	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
DC Gain Drift G = +1	$\Delta G/\Delta T_A$	—	±1	—	ppm/°C	T_A = -40°C to +125°C
G ≥ +10	$\Delta G/\Delta T_A$	—	±4	—	ppm/°C	T_A = -40°C to +1285°C
Ladder Resistance (Note 1)						
Ladder Resistance	R_{LAD}	200	350	500	kΩ	
Ladder Resistance across Temperature	$\Delta R_{LAD}/\Delta T_A$	—	–1800	—	ppm/°C	T_A = -40°C to +125°C
Amplifier Output						
DC Output Non-linearity G = +1	V_{ONL}	–0.2	—	+0.2	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 1.8V
	V_{ONL}	–0.1	—	+0.1	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 5.5V
DC Output Non-linearity, G = +10, +50	V_{ONL}	–0.05	—	+0.05	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V
Maximum Output Voltage Swing	V_{OH}, V_{OL}	V_{SS}+10	—	V_{DD}–10	mV	G = +1; 0.3V output overdrive
	V_{OH}, V_{OL}	V_{SS}+10	—	V_{DD}–10	mV	G ≥ +10; 0.5V output overdrive
Short Circuit Current	I_{SC}	—	±7	—	mA	V_{DD} = 1.8V
	I_{SC}	—	±20	—	mA	V_{DD} = 5.5V

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{SS}, V_{OUT}, and the inverting input of the internal amplifier. Thus, V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 0.6 µA at V_{OUT} = 0.3V), and excludes digital switching currents.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	60	110	170	µA	I_O = 0 **(Note 2)**

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{SS}, V_{OUT}, and the inverting input of the internal amplifier. Thus, V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 0.6 µA at V_{OUT} = 0.3V), and excludes digital switching currents.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
-3dB Bandwidth	BW	—	900	—	kHz	G = +1, V_{OUT} < 100 mV_{P-P} **(Note 1)**
	BW	—	350	—	kHz	G = +10, V_{OUT} < 100 mV_{P-P} **(Note 1)**
	BW	—	250	—	kHz	G = +50, V_{OUT} < 100 mV_{P-P} **(Note 1)**
Gain Peaking	GPK	—	0.3	—	dB	G = +1; V_{OUT} < 100 mV_{P-P}
	GPK	—	0	—	dB	G = +10, V_{OUT} < 100 mV_{P-P}
	GPK	—	0.7	—	dB	G = +50; V_{OUT} < 100 mV_{P-P}
Total Harmonic Distortion plus Noise						
f = 1 kHz, G = +1 V/V	THD+N	—	0.0029	—	%	V_{OUT} = 1.75V ± $1.4V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
f = 1 kHz, G = +10 V/V	THD+N	—	0.18	—	%	V_{OUT} = 2.5V ± $1.4V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
f = 1 kHz, G = +50 V/V	THD+N	—	1.3	—	%	V_{OUT} = 2.5V ± $1.4V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
Step Response						
Slew Rate	SR	—	0.50	—	V/µs	G = 1
	SR	—	2.3	—	V/µs	G = 10
	SR	—	4.5	—	V/µs	G = 50
Noise						
Input Noise Voltage	E_{ni}	—	9	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz **(Note 2)**
	E_{ni}	—	50	—	$µV_{P-P}$	f = 0.1 Hz to 30 kHz **(Note 2)**
Input Noise Voltage Density	e_{ni}	—	38	—	nV/√Hz	G = +1 V/V, f = 10 kHz **(Note 2)**
	e_{ni}	—	46	—	nV/√Hz	G = +10 V/V, f = 10 kHz **(Note 2)**
	e_{ni}	—	41	—	nV/√Hz	G = +50 V/V, f = 10 kHz **(Note 2)**
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 10 kHz

Note 1: See Table 4-1 for a list of typical numbers and Figure 2-31 for the frequency response versus gain.

2: E_{ni} and e_{ni} include ladder resistance thermal noise.

DIGITAL ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{CSL}	0	—	$0.2V_{DD}$	V	$\overline{CS}$ = 0V
$\overline{CS}$ Input Current, Low	I_{CSL}	—	30	—	pA	$\overline{CS}$ = 0V
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{CSH}	$0.8V_{DD}$	—	V_{DD}	V	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.8	—	µA	$\overline{CS}$ = V_{DD} = 5.5V
Quiescent Current per Amplifier, Shutdown Mode (I_{DD})	I_{DD_SHDN}	—	120	—	pA	$\overline{CS}$ = V_{DD}, MCP6G03
Quiescent Current per Amplifier, Shutdown Mode (I_{SS}) **(Note 3)**	I_{SS_SHDN}	—	–2.4	—	µA	$\overline{CS}$ = V_{DD} = 1.8V, MCP6G03
	I_{SS_SHDN}	—	–7.2	—	µA	$\overline{CS}$ = V_{DD} = 5.5V, MCP6G03
$\overline{CS}$ Dynamic Specifications						
Input Capacitance	C_{CS}	—	10	—	pF	
Input Rise/Fall Times	t_{CSRF}	—	—	2	µs	**(Note 2)**
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{CSON}	—	40	—	µs	G = +1 V/V, V_{DD} = 1.8V, V_{IN} = $0.9V_{DD}$ $\overline{CS}$ = $0.2V_{DD}$ to V_{OUT} = $0.8V_{DD}$
	t_{CSON}	—	7	—	µs	G = +1 V/V, V_{DD} = 5.5V, V_{IN} = $0.9V_{DD}$ $\overline{CS}$ = $0.2V_{DD}$ to V_{OUT} = $0.8V_{DD}$
$\overline{CS}$ High to Amplifier Output High-Z Turn-off Time	t_{CSOFF}	—	30	—	µs	G = +1 V/V, V_{IN} = V_{DD}/2, $\overline{CS}$ = $0.8V_{DD}$ to V_{OUT} = $0.1V_{DD}$/2
Hysteresis	V_{CSHY}	—	0.40	—	V	V_{DD} = 1.8V
	V_{CSHY}	—	0.55	—	V	V_{DD} = 5.5V
GSEL Specifications (Note 1)						
GSEL Logic Threshold, Low	V_{GSL}	$0.15V_{DD}$	—	$0.35V_{DD}$	V	Gain changes between 1 and 10, I_{GSEL} = 0
GSEL Logic Threshold, High	V_{GSH}	$0.65V_{DD}$	—	$0.85V_{DD}$	V	Gain changes between 1 and 50, I_{GSEL} = 0
GSEL Input Current, Low	I_{GSL}	–10	—	–1.5	µA	GSEL voltage = $0.3V_{DD}$
GSEL Input Current, High	I_{GSH}	+1.5	—	+10	µA	GSEL voltage = $0.7V_{DD}$
GSEL Dynamic Specifications (Note 1)						
Input Capacitance	C_{GSEL}	—	8	—	pF	
Input Rise/Fall Times	t_{GSRF}	—	—	10	µs	**(Note 2)**
Hysteresis	V_{GSHY}	—	45	—	mV	V_{DD} = 1.8V
	V_{GSHY}	—	95	—	mV	V_{DD} = 5.5V
GSEL Low to Valid Output Time, G = +1 to +10 Select	t_{GSL1}	—	10	—	µs	V_{IN} = 150 mV, GSEL = $0.25V_{DD}$ to V_{OUT} = 1.37V
GSEL Middle to Valid Output Time, G = +10 to +1 Select	t_{GSM10}	—	12	—	µs	V_{IN} = 150 mV, GSEL = $0.25V_{DD}$ to V_{OUT} = 0.28V
GSEL High to Valid Output Time, G = +1 to +50 Select	t_{GSH1}	—	9	—	µs	V_{IN} = 30 mV, GSEL = $0.75V_{DD}$ to V_{OUT} = 1.35V
GSEL Middle to Valid Output Time, G = +50 to +1 Select	t_{GSM50}	—	8	—	µs	V_{IN} = 30 mV, GSEL = $0.75V_{DD}$ to V_{OUT} = 0.18V

Note 1: GSEL is a tri-level input pin. The gain is 10 when its voltage is low, 1 when it is at mid-suppy, and 50 when it is high.

2: Not tested in production. Set by design and characterization.

3: I_{SS_SHDN} includes the current through the $\overline{CS}$ pin, R_L and R_{LAD}, and excludes digital switching currents. The block diagram on the from page shows these current paths (through V_{SS}).

DIGITAL ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise indicated, T_A = 25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to $V_{DD}/2$, C_L = 60 pF, GSEL = $V_{DD}/2$, and $\overline{CS}$ is tied low.						
GSEL High to Valid Output Time, G = +10 to +50 Select	t_{GSH10}	—	12	—	µs	V_{IN} = 30 mV, GSEL = $0.75V_{DD}$ to V_{OUT} = 1.38V
GSEL Low to Valid Output Time, G = +50 to +10 Select	t_{GSL50}	—	9	—	µs	V_{IN} = 30 mV, GSEL = $0.25V_{DD}$ to V_{OUT} = 0.42V

Note 1: GSEL is a tri-level input pin. The gain is 10 when its voltage is low, 1 when it is at mid-suppy, and 50 when it is high.
2: Not tested in production. Set by design and characterization.
3: I_{SS_SHDN} includes the current through the $\overline{CS}$ pin, R_L and R_{LAD}, and excludes digital switching currents. The block diagram on the from page shows these current paths (through V_{SS}).

TEMPERATURE CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, and V_{SS} = GND.						
Temperature Ranges						
Specified Temperature Range	T_A	–40	—	+125	°C	
Operating Temperature Range	T_A	–40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	–65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP6G01/2/3/4 family of SGAs operates over this temperature range, but operation must not cause T_J to exceed Maximum Junction Temperature (+150°C).

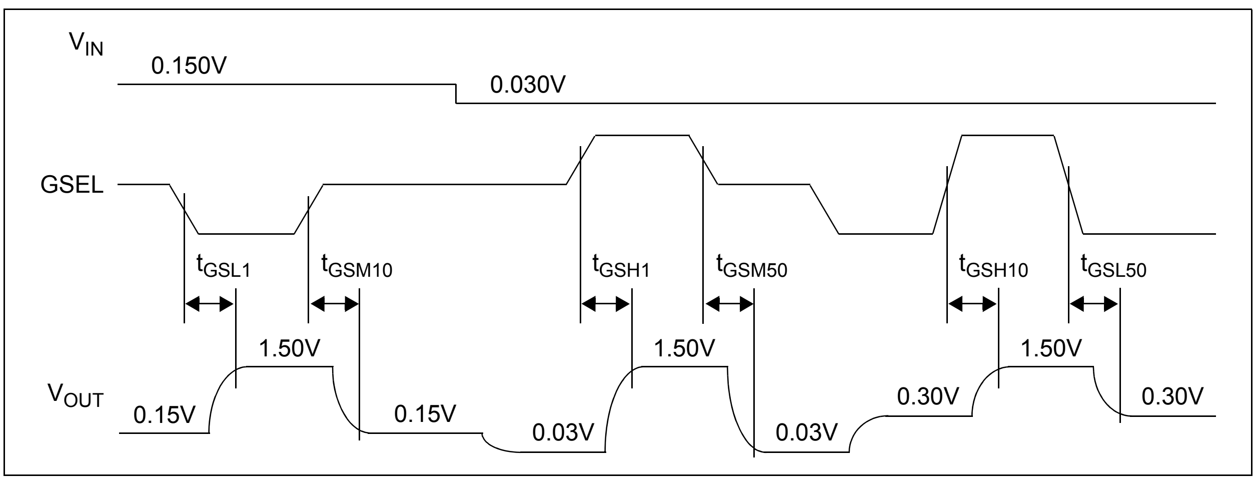


FIGURE 1-1: *Gain Select Timing Diagram.*

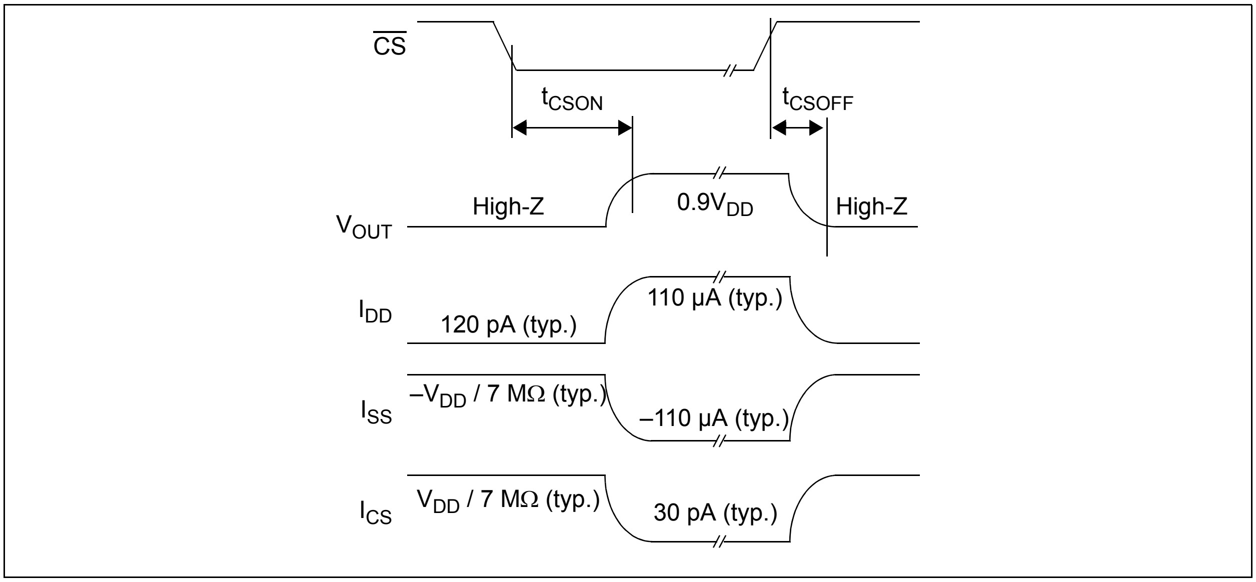


FIGURE 1-2: *SGA Chip Select Timing Diagram.*

1.1 DC Output Voltage Specs / Model

1.1.1 IDEAL MODEL

The ideal SGA output voltage (V_{OUT}) is (see Figure 1-3):

EQUATION 1-1:

$$V_{O\_ID} = GV_{IN}$$

Where:

G is the nominal gain

$$V_{REF} = V_{SS} = 0\text{V}$$

This equation holds when there are no gain or offset errors.

1.1.2 LINEAR MODEL

The SGA's linear region of operation is modeled by the line V_{O_LIN} shown in Figure 1-3. V_{O_LIN} includes offset and gain errors, but does not include non-linear effects.

EQUATION 1-2:

$$V_{O\_LIN} = G(1 + g_E)\left(V_{IN} - \frac{0.3\text{V}}{G} + V_{OS}\right) + 0.3\text{V}$$

Where:

G is the nominal gain

g_E is the gain error

V_{OS} is the input offset voltage

$$V_{REF} = V_{SS} = 0\text{V}$$

This line's endpoints are 0.3V from the supply rails (V_{O_ID} = 0.3V and V_{DD} – 0.3V). The gain error and input offset voltage specifications (in the electrical specifications) relate to Figure 1-3 as follows:

EQUATION 1-3:

$$g_E = 100\% \cdot \frac{V_2 - V_1}{V_{DD} - 0.6\text{V}}$$

$$V_{OS} = \frac{V_1}{G(1 + g_E)}, \quad G = +1$$

Where:

$$V_1 = V_{OUT} - V_{O\_ID}, \quad V_{O\_ID} = 0.3\text{V}$$

$$V_2 = V_{OUT} - V_{O\_ID}, \quad V_{O\_ID} = V_{DD} - 0.3\text{V}$$

The input offset specification describes V_{OS} at G = +1 V/V.

The DC Gain Drift ($\Delta G/\Delta T_A$) can be calculated from the change in g_E across temperature. This is shown in the following equation:

EQUATION 1-4:

$$\Delta G/\Delta T_A = G \cdot \frac{\Delta g_E}{\Delta T_A}, \quad \text{in units of V/V/°C}$$

$$\Delta G/\Delta T_A = 100\% \cdot \frac{\Delta g_E}{\Delta T_A}, \quad \text{in units of \%/°C}$$

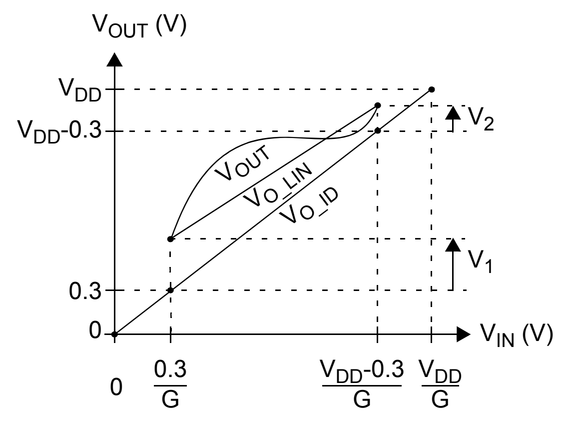


FIGURE 1-3: *Output Voltage Model.*

1.1.3 OUTPUT NON-LINEARITY

Figure 1-4 shows the Integral Non-Linearity (INL) of the output voltage. INL is the output non-linearity error not explained by V_{O_LIN}:

EQUATION 1-5:

$$INL = V_{OUT} - V_{O\_LIN}$$

The output non-linearity specification (in the Electrical Specifications, with units of % of FSR) is related to Figure 1-4 by:

EQUATION 1-6:

$$V_{ONL} = 100\% \cdot \frac{max(V_3, V_4)}{V_{DD} - 0.6\text{V}}$$

Where:

$$V_3 = max(-INL)$$

$$V_4 = max(INL)$$

Note that the Full Scale Range (FSR) is V_{DD} – 0.6V (0.3V to V_{DD} – 0.3V).

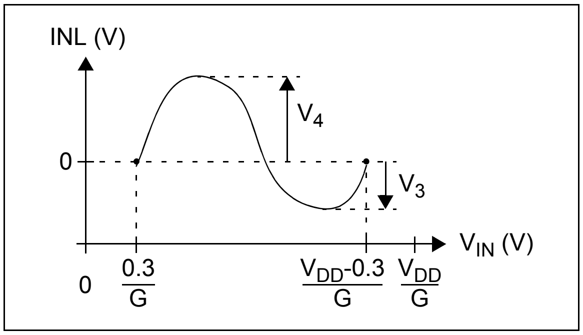


FIGURE 1-4: *Output Voltage INL.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

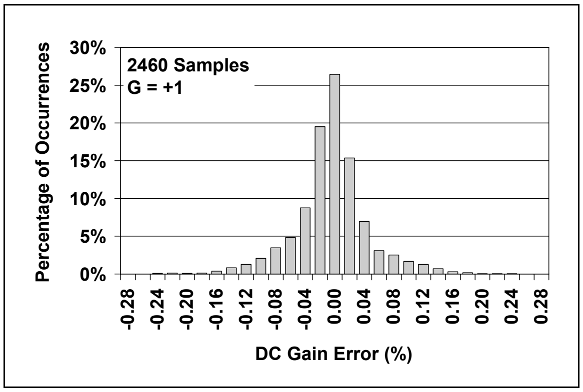


FIGURE 2-1: *DC Gain Error, G = +1.*

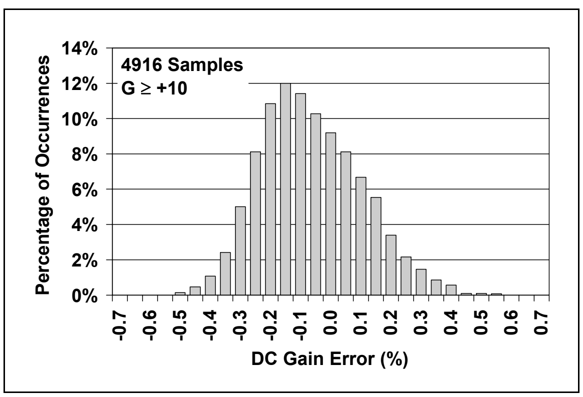


FIGURE 2-2: *DC Gain Error, G ≥ +10.*

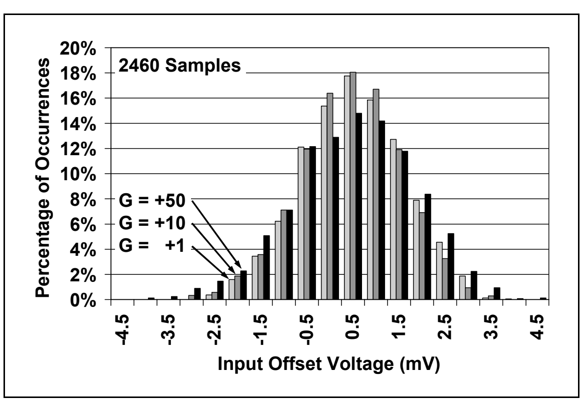


FIGURE 2-3: *Input Offset Voltage.*

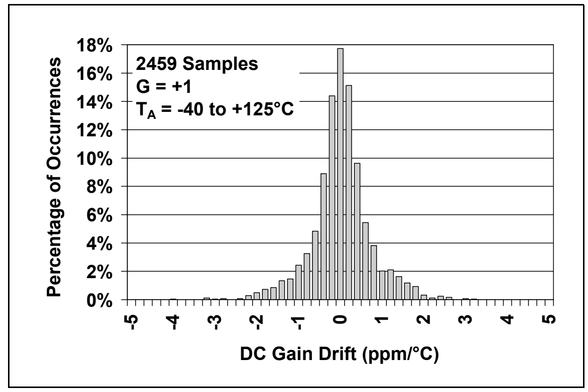


FIGURE 2-4: *DC Gain Drift, G = +1.*

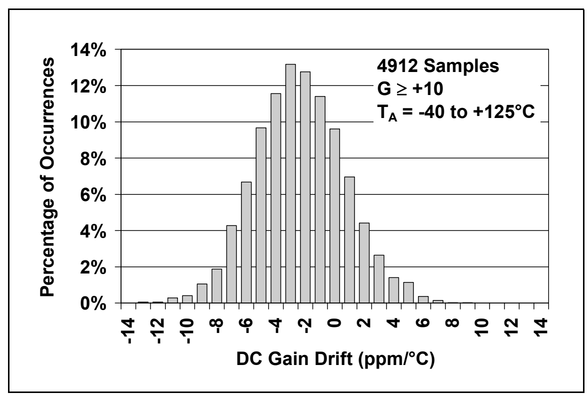


FIGURE 2-5: *DC Gain Drift, G ≥ +10.*

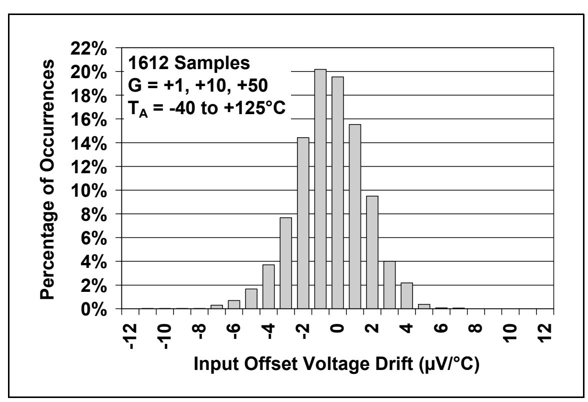


FIGURE 2-6: *Input Offset Voltage Drift.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

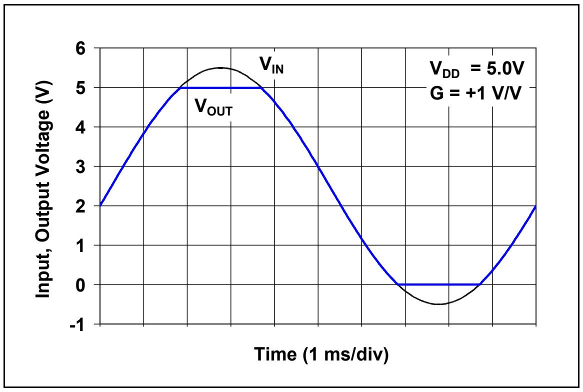


FIGURE 2-7: *The MCP6G01/2/3/4 family shows no phase reversal under overdrive.*

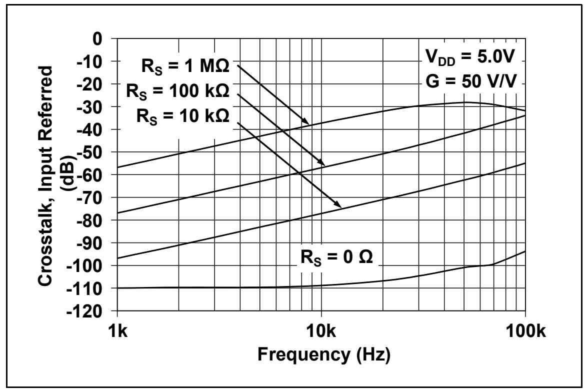


FIGURE 2-10: *Crosstalk vs. Frequency, with G = 50 (circuit in Figure 4-7).*

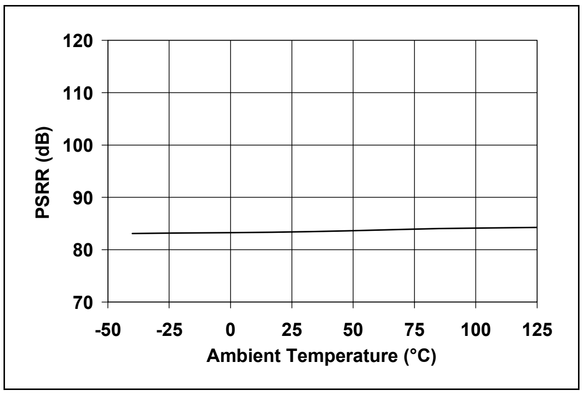


FIGURE 2-8: *PSRR vs. Temperature.*

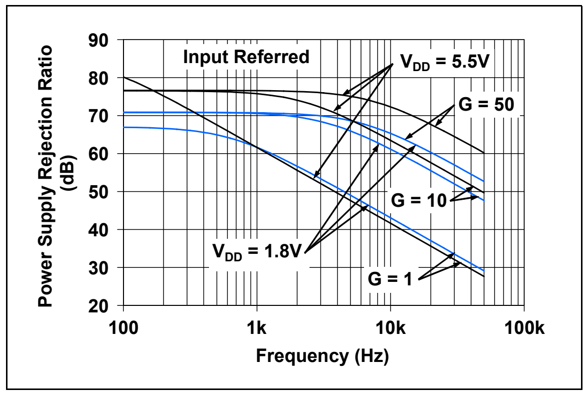


FIGURE 2-11: *PSRR vs. Frequency.*

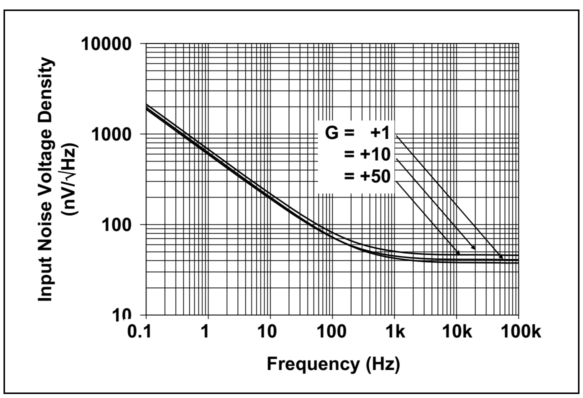


FIGURE 2-9: *Input Noise Voltage Density vs. Frequency.*

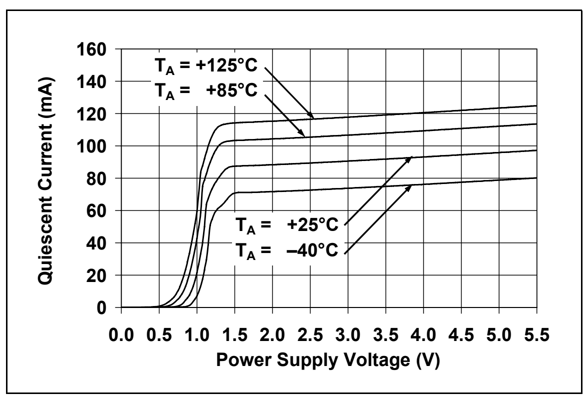


FIGURE 2-12: *Quiescent Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

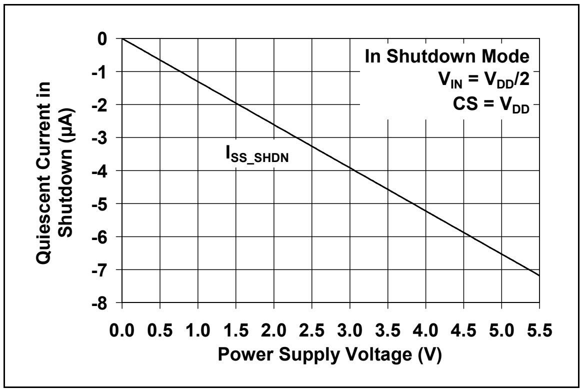


FIGURE 2-13: *Quiescent Current (I_{SS}) in Shutdown Mode vs. Supply Voltage.*

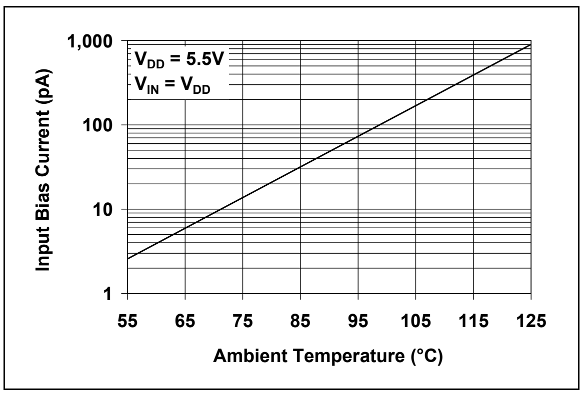


FIGURE 2-14: *Input Bias Current vs. Temperature.*

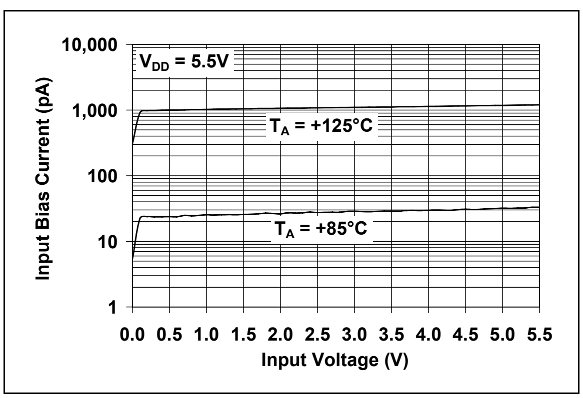


FIGURE 2-15: *Input Bias Current vs. Input Voltage.*

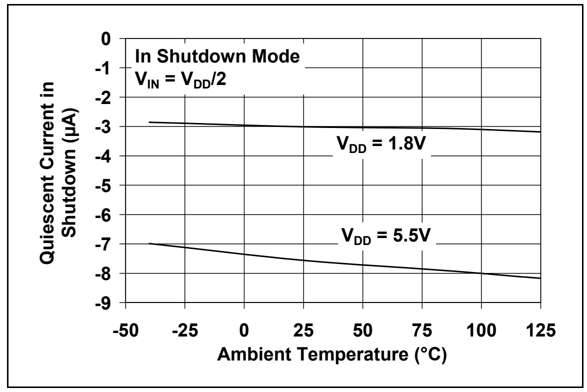


FIGURE 2-16: *Quiescent Current (I_{SS}) in Shutdown Mode vs. Temperature.*

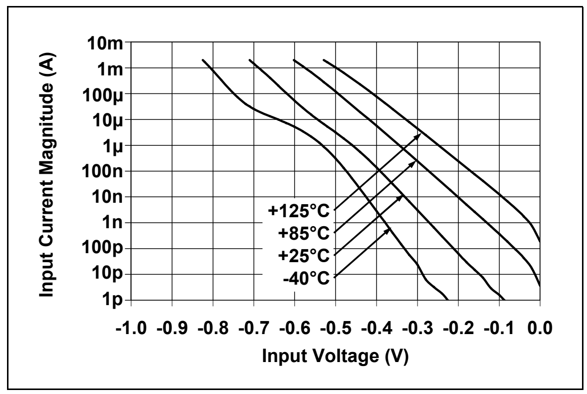


FIGURE 2-17: *Input Bias Current vs. Input Voltage.*

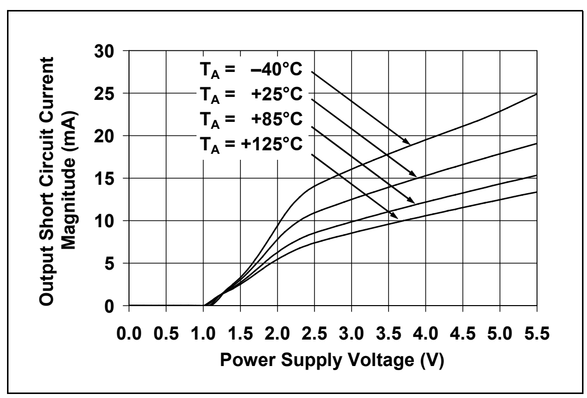


FIGURE 2-18: *Output Short Circuit Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and CS is tied low.

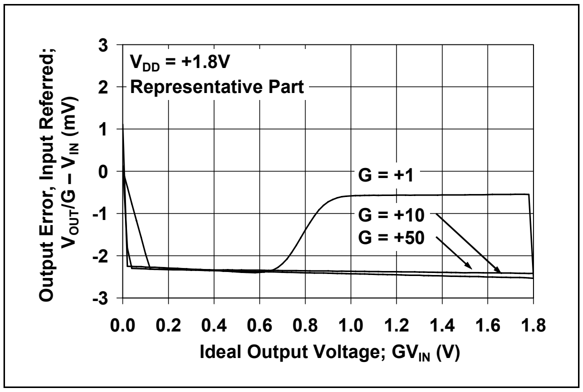


FIGURE 2-19: Output Voltage Error vs. Ideal Output Voltage, with V_{DD} = 1.8V.

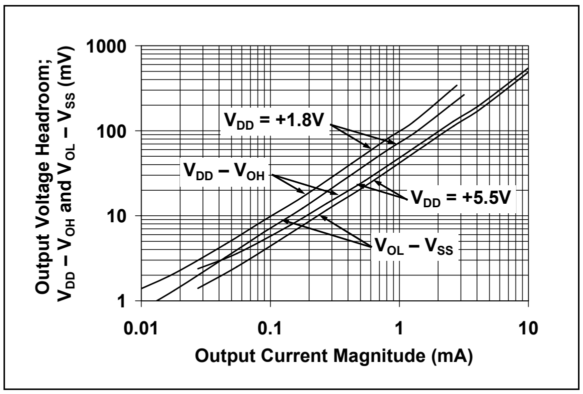


FIGURE 2-20: Output Voltage Headroom vs. Output plus Ladder Current (circuit in Figure 4-4).

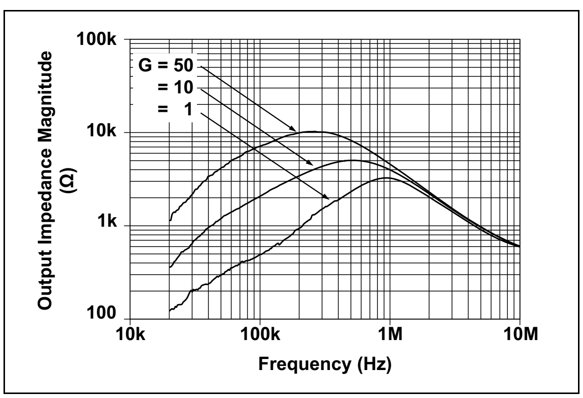


FIGURE 2-21: Output Impedance vs. Frequency.

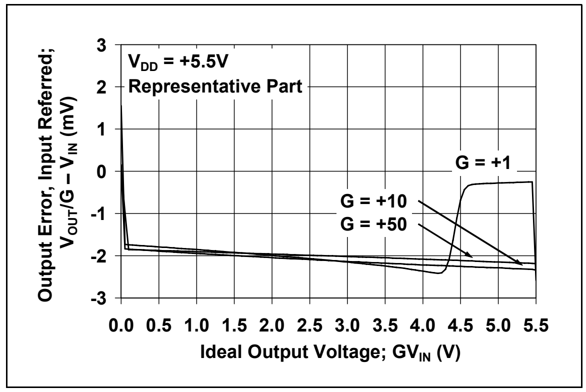


FIGURE 2-22: Output Voltage Error vs. Ideal Output Voltage, with V_{DD} = 5.5V.

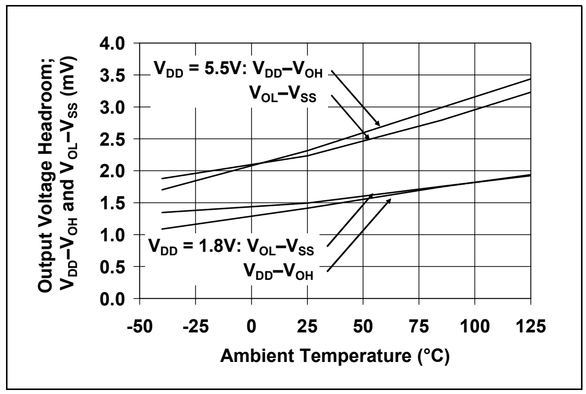


FIGURE 2-23: Output Voltage Headroom vs. Temperature.

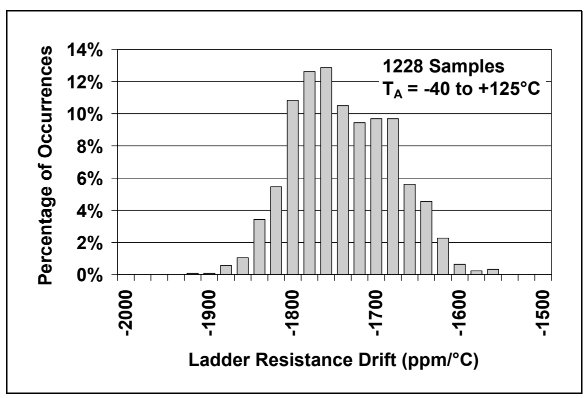


FIGURE 2-24: Ladder Resistance Drift.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

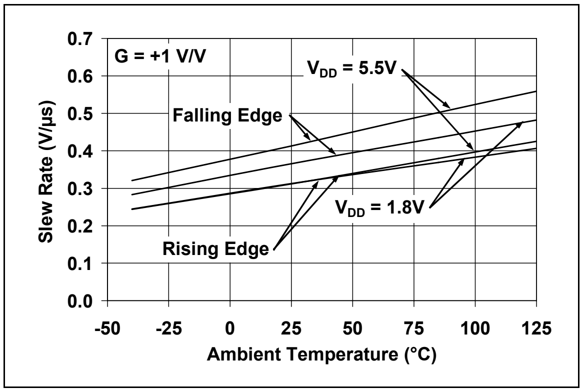


FIGURE 2-25: *Slew Rate vs. Temperature, with G = +1.*

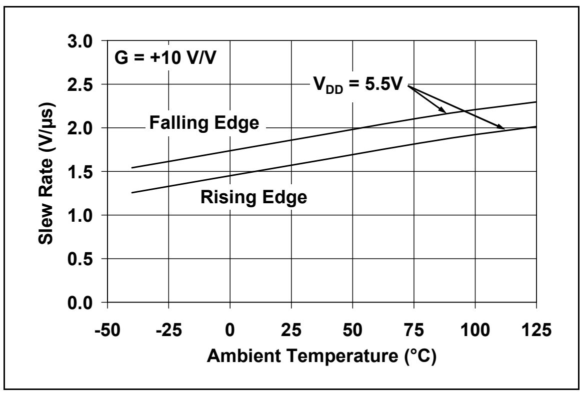


FIGURE 2-26: *Slew Rate vs. Temperature, with G = +10.*

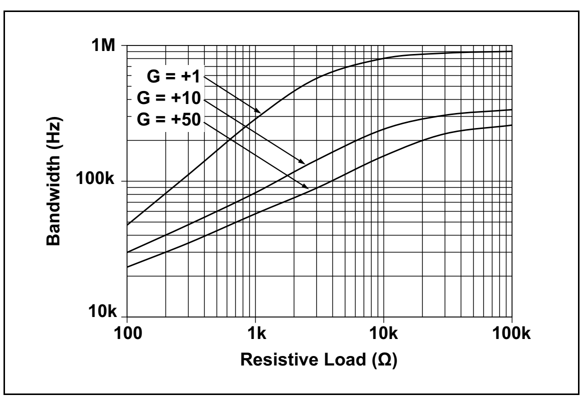


FIGURE 2-27: *Bandwidth vs. Resistive Load.*

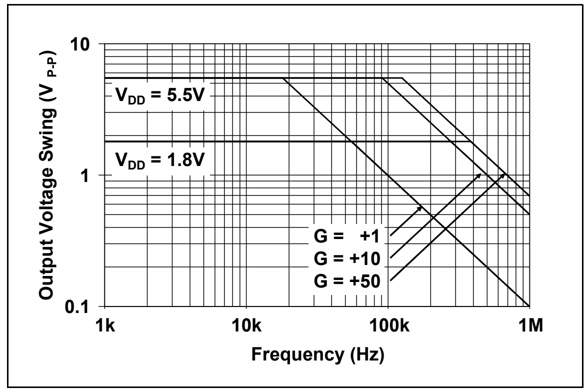


FIGURE 2-28: *Output Voltage Swing vs. Frequency.*

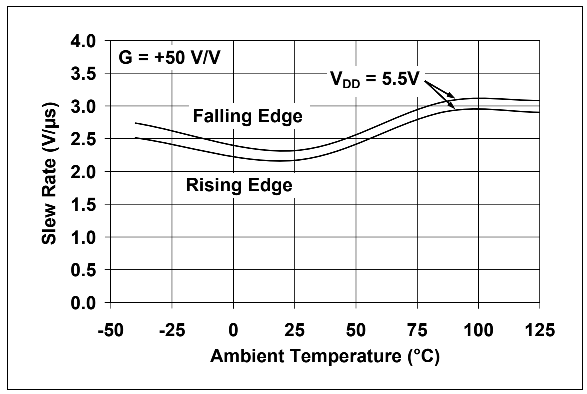


FIGURE 2-29: *Slew Rate vs. Temperature, with G = +50.*

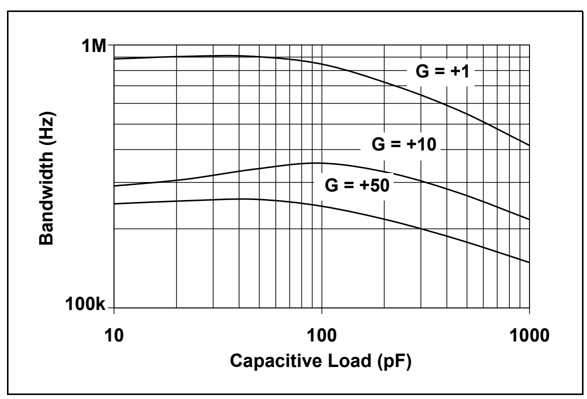


FIGURE 2-30: *Bandwidth vs. Capacitive Load.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to $V_{DD}/2$, C_L = 60 pF, GSEL = $V_{DD}/2$, and $\overline{CS}$ is tied low.

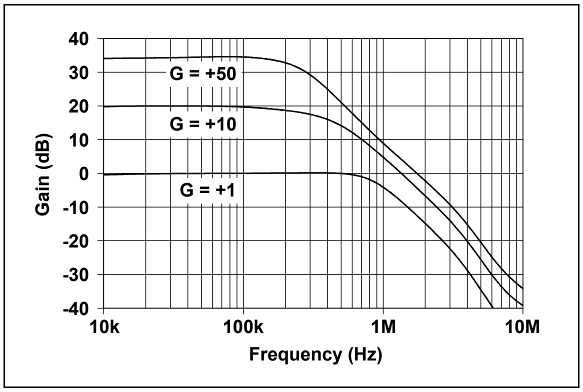


FIGURE 2-31: *Gain vs. Frequency.*

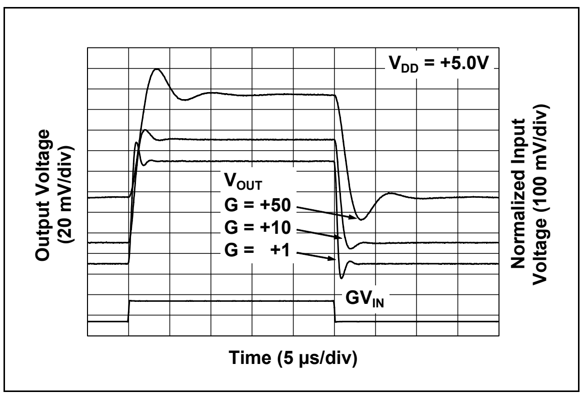


FIGURE 2-32: *Small Signal Pulse Response.*

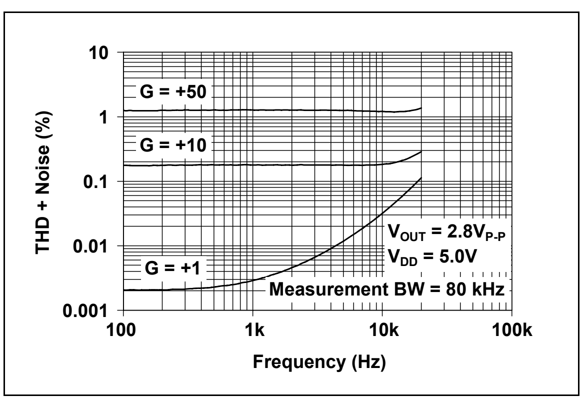


FIGURE 2-33: *THD plus Noise vs. Frequency, V_{OUT} = 2.8 V_{P-P}*

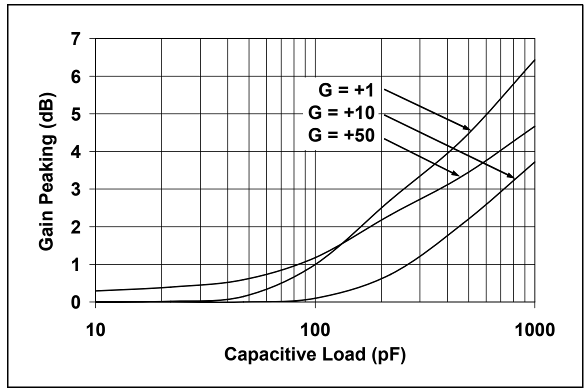


FIGURE 2-34: *Gain Peaking vs. Capacitive Load.*

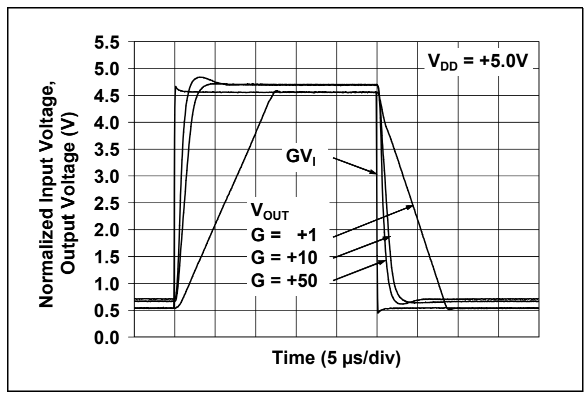


FIGURE 2-35: *Large Signal Pulse Response.*

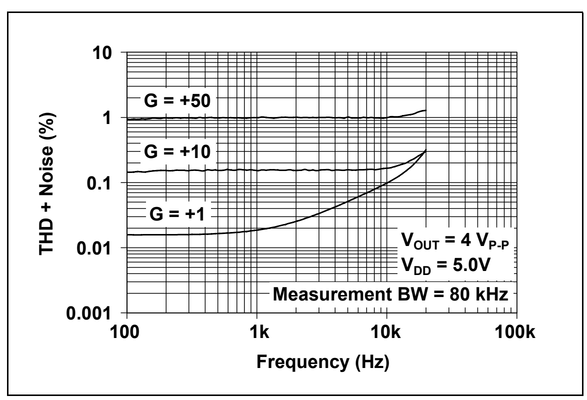


FIGURE 2-36: *THD plus Noise vs. Frequency, V_{OUT} = 4.0 V_{P-P}*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

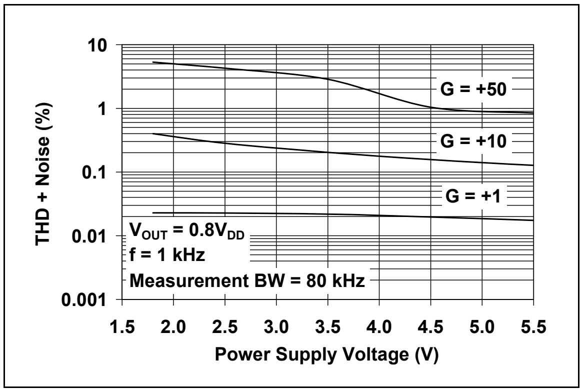


FIGURE 2-37: *THD plus Noise vs. Supply Voltage.*

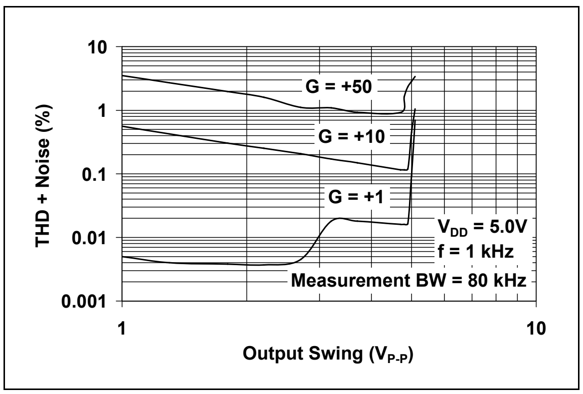


FIGURE 2-38: *THD plus Noise vs. Output Swing.*

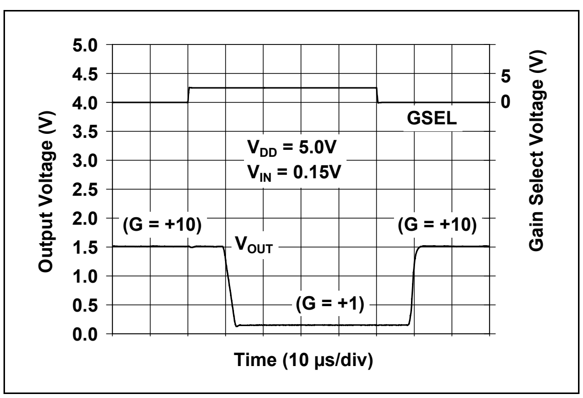


FIGURE 2-39: *Gain Select Timing, with Gain = 1 and 10.*

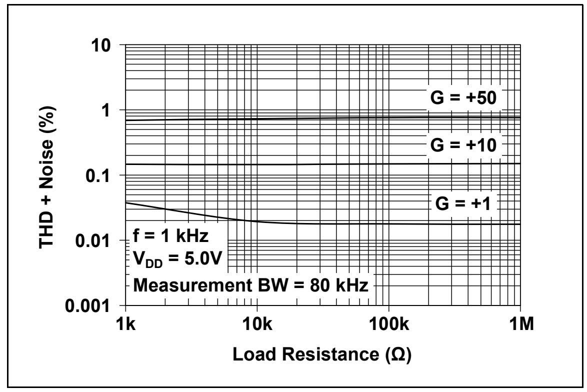


FIGURE 2-40: *THD plus Noise vs. Load Resistance.*

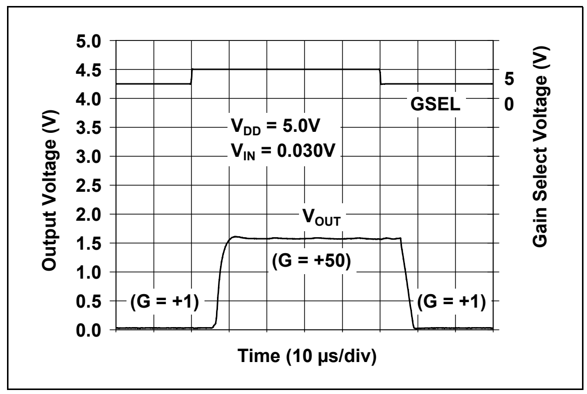


FIGURE 2-41: *Gain Select Timing, with Gain = 1 and 50.*

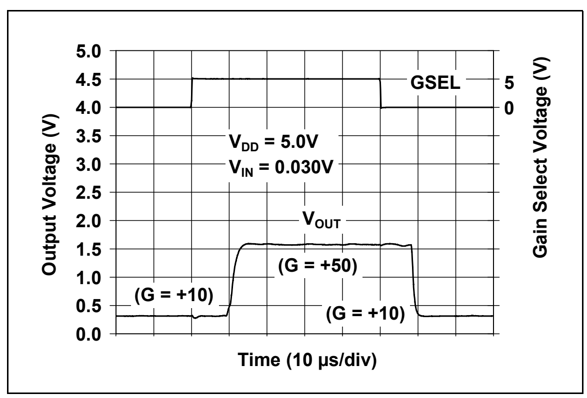


FIGURE 2-42: *Gain Select Timing, with Gain = 1 and 10.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

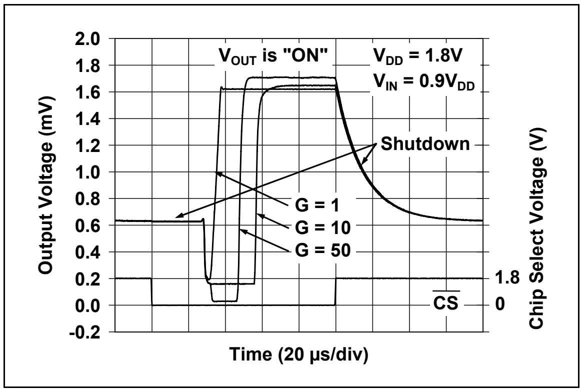


FIGURE 2-43: Output Voltage vs. Chip Select, with V_{DD} = 1.8V.

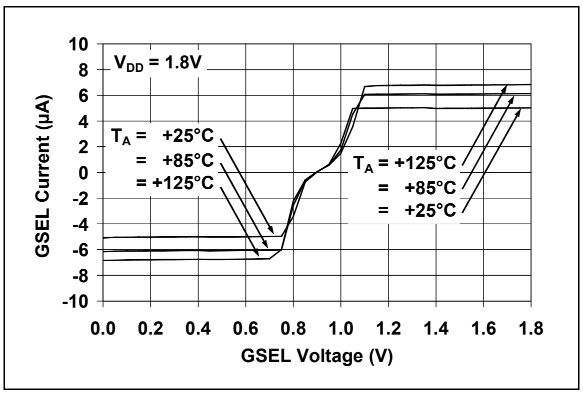


FIGURE 2-44: GSEL Pin Current vs. GSEL Voltage, with V_{DD} = 1.8V.

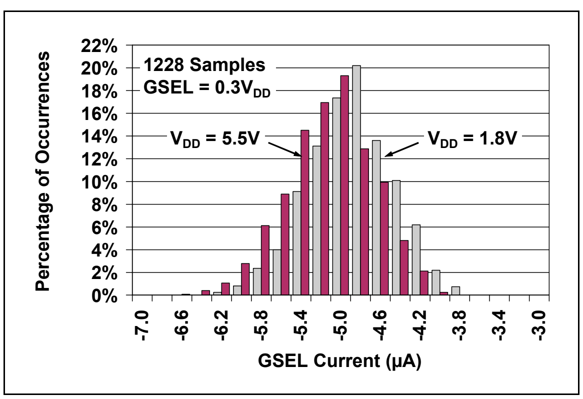


FIGURE 2-45: GSEL Current, with GSEL Voltage of 0.3V_{DD}.

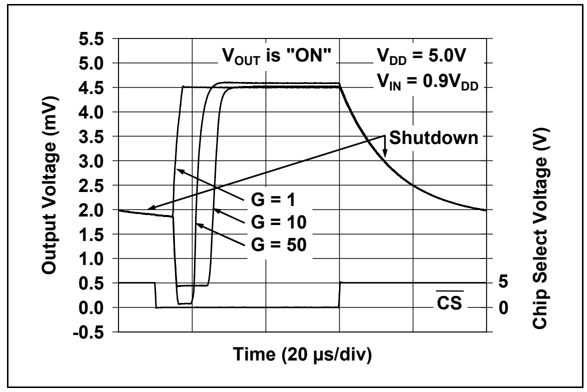


FIGURE 2-46: Output Voltage vs. Chip Select, with V_{DD} = 5.0V.

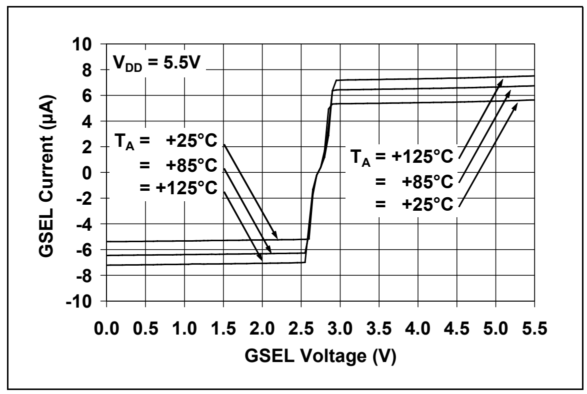


FIGURE 2-47: GSEL Pin Current vs. GSEL Voltage, with V_{DD} = 5.5V.

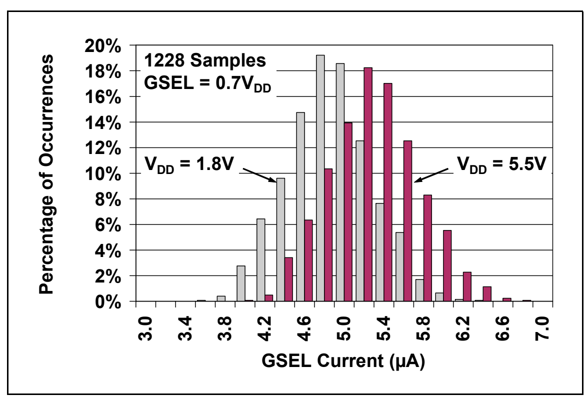


FIGURE 2-48: GSEL Current, with GSEL Voltage of 0.7V_{DD}.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, G = +1 V/V, V_{IN} = (0.3V)/G, R_L = 100 kΩ to V_{DD}/2, C_L = 60 pF, GSEL = V_{DD}/2, and $\overline{CS}$ is tied low.

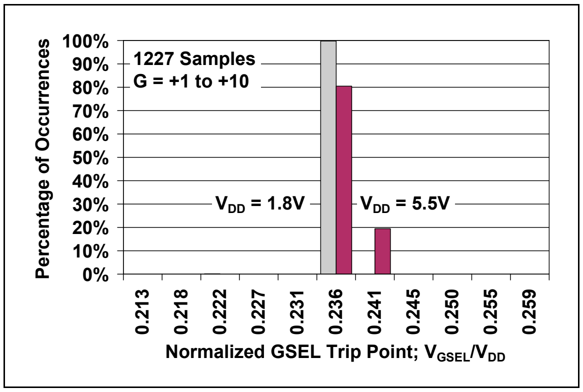


FIGURE 2-49: *GSEL Trip Point between G = +1 and G = +10.*

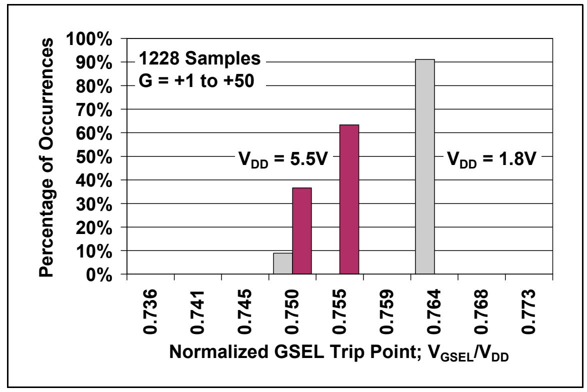


FIGURE 2-50: *GSEL Trip Point between G = +1 and G = +50.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6G01	MCP6G02	MCP6G03	MCP6G04	Symbol	Description
6	1	6	1	V_{OUT}, V_{OUTA}	Analog Output (SGA A)
2	2	2	2	GSEL, GSELA	Gain Select Input (SGA A)
3	3	3	3	V_{IN}, V_{INA}	Analog Input (SGA A)
7	8	7	4	V_{DD}	Positive Power Supply
—	5	—	5	V_{INB}	Analog Input (SGA B)
—	6	—	6	GSELB	Gain Select Input (SGA B)
—	7	—	7	V_{OUTB}	Analog Output (SGA B)
—	—	—	8	V_{OUTC}	Analog Output (SGA C)
—	—	—	9	GSELC	Gain Select Input (SGA C)
—	—	—	10	V_{INC}	Analog Input (SGA C)
4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	12	V_{IND}	Analog Input (SGA D)
—	—	—	13	GSELD	Gain Select Input (SGA D)
—	—	—	14	V_{OUTD}	Analog Output (SGA D)
—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	1, 5	—	NC	No Internal Connection

3.1 Analog Output

The output pin (V_{OUT}) is a low impedance voltage source. The selected gain (G) and input voltage (V_{IN}) determine its value.

3.2 Analog Input

The analog inputs (V_{IN}) are high impedance CMOS inputs with low bias currents. Only three fixed, non-inverting gains are available through these inputs.

3.3 Power Supply (V_{SS} and V_{DD})

The Positive Power Supply Pin (V_{DD}) is 1.8V to 5.5V higher than the Negative Power Supply Pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground, and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These parts need to use a bulk capacitor (typically 1.0 µF to 10 µF) within 100 mm of the V_{DD} pin; it can be shared with nearby analog parts.

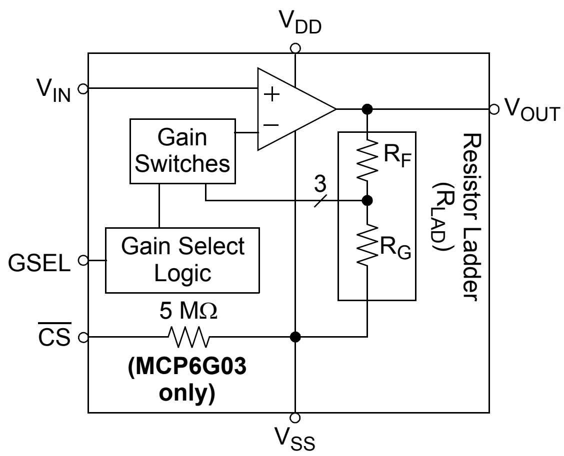
3.4 Digital Inputs

The Chip Select ($\overline{CS}$) input is a Schmitt-triggered, CMOS logic input.

The Gain Select (GSEL) inputs are tri-level digital inputs. They function similar to normal logic inputs at low (G = +10) and high voltages (G = +50). The pin can also be set to mid-supply (G = +1) by a low impedance source, or by leaving this pin open.

4.0 APPLICATIONS INFORMATION

The MCP6G01/2/3/4 family of Selectable Gain Amplifiers (SGA) is based on simple analog building blocks (see Figure 4-1). Each of these blocks will be explained in more detail in the following subsections.



Gain (V/V)	GSEL Voltage (Typ.) (V)
1	V_{DD}/2 (or open)
10	0
50	V_{DD}

Note: V_{SS} is assumed to be 0V

FIGURE 4-1: *SGA Block Diagram.*

4.1 Internal Op Amp

The internal op amp gives the right combination of bandwidth, accuracy, and flexibility.

4.1.1 COMPENSATION CAPACITORS

The internal op amp has three compensation capacitors (comp. caps.) connected to a switching network. They are selected to give good small signal bandwidth at high gains, and good slew rate (full power bandwidth) at low gains. The change in bandwidth as gain changes is between 250 and 900 kHz. Refer to Table 4-1 for more information.

TABLE 4-1: GAIN VS. INTERNAL COMPENSATION CAPACITOR

Gain (V/V)	Internal Comp. Cap.	G x BW (MHz) Typ.	SR (V/µs) Typ.	FPBW (kHz) Typ.	BW (kHz) Typ.
1	Large	0.90	0.50	29	900
10	Medium	3.5	2.3	133	350
50	Small	12.5	4.5	260	250

Note 1: Changing the compensation capacitor does not change the DC performance (e.g., V_{OS}).
2: G x BW is approximately the Gain Bandwidth Product of the internal op amp.
3: FPBW is the Full Power Bandwidth at V_{DD} = 5.5V, which is based on slew rate (SR).
4: BW is the closed-loop, small signal –3 dB bandwidth.

4.1.2 RAIL-TO-RAIL INPUTS

The input stage of the internal op amp uses two differential input stages in parallel; one operates at low V_{IN} (input voltage), while the other operates at high V_{IN}. With this topology, the internal inputs can operate to 0.3V past either supply rail, although the output will clip the signal before that happens.

The transition between the two input stage occurs when $V_{IN} \approx V_{DD} - 1.1V$ (see Figure 2-19 and Figure 2-22). For the best distortion and gain linearity, avoid this region of operation.

4.1.3 PHASE REVERSAL

The MCP6G01/2/3/4 amplifier family is designed with CMOS input devices. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-7 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.1.4 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass ESD events within the specified limits.

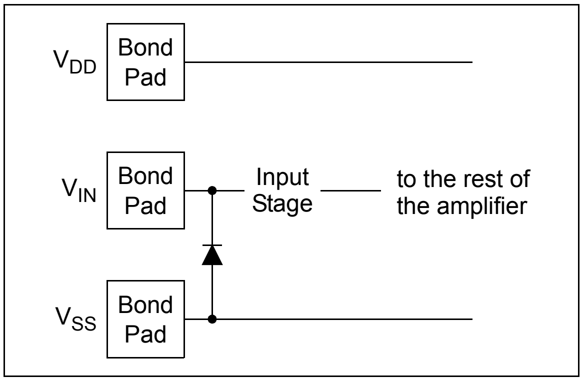


FIGURE 4-2: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the V_{IN} pins (see **Section "Absolute Maximum Ratings †"** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}) from going too far below ground, and the resistor R_1 limits the possible current drawn out of the input pin. Diode D_1 prevents the input pin (V_{IN}) from going too far above V_{DD}. When implemented as shown, resistor R_1 also limits the current through D_1.

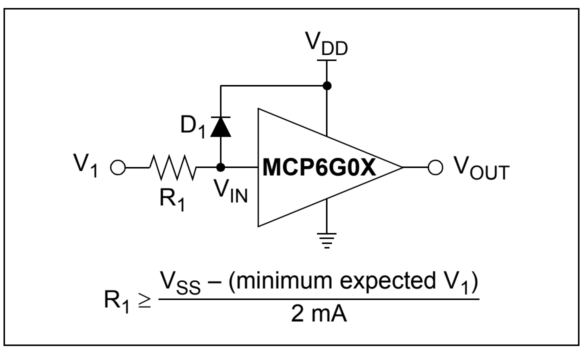


FIGURE 4-3: *Protecting the Analog Inputs.*

It is also possible to connect the diode to the left of the resistor R_1. In this case, the current through the diode D_1 needs to be limited by some other mechanism. The resistor then serves as in-rush current limiter; the DC current into the input pin (V_{IN}) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-17. Applications that are high impedance may need to limit the useable voltage range.

4.1.5 RAIL-TO-RAIL OUTPUT

The maximum output voltage swing is the maximum swing possible under a particular amplifier load current. The amplifier load current is the sum of the external load current (I_{OUT}) and the current through the ladder resistance (I_{LAD}); see Figure 4-4.

EQUATION 4-1:

$$Amplifier\ Load\ Current = I_{OUT} + I_{LAD}$$

Where:

$$I_{LAD} = \frac{(V_{OUT} - V_{SS})}{R_{LAD}}$$

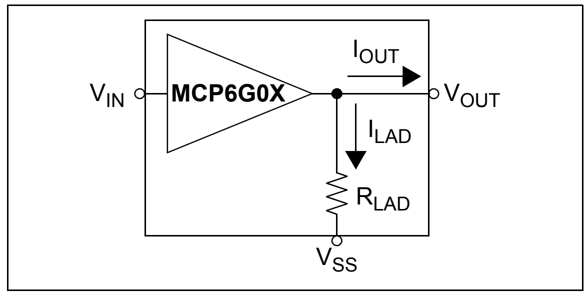


FIGURE 4-4: *Amplifier Load Current.*

See Figure 2-20 for the typical output headroom ($V_{DD} – V_{OH}$ or $V_{OL} – V_{SS}$) as a function of amplifier load current. The specification table states the output can reach within 10 mV of either supply rail when R_L = 100 kΩ.

4.2 Resistor Ladder

The resistor ladder shown in Figure 4-1 ($R_{LAD} = R_F + R_G$) sets the gain. Placing the gain switches in series with the inverting input reduces the parasitic capacitance, distortion, and gain mismatch.

R_{LAD} is an additional load on the output of the SGA and causes additional current draw from the supplies.

When $\overline{CS}$ is high, the SGA is shut down (low power). R_{LAD} is still attached to the V_{OUT} and V_{SS} pins. Thus, these pins and the internal amplifier's inverting input are all connected through R_{LAD} and the output is not high-Z (unlike the internal op amp).

R_{LAD} contributes to the output noise; see Figure 2-9.

R_{LAD} is intended to be driven at the V_{SS} pin by a low impedance voltage source. The power supply driving the V_{SS} pin should have an output impedance less than 0.1Ω to maintain reasonable gain accuracy.

4.3 MCP6G03 Chip Select ($\overline{CS}$)

The MCP6G03 is a single amplifier with chip select ($\overline{CS}$). When $\overline{CS}$ is high, the internal op amp is shut down and its output placed in a high-Z state. The resistive ladder is always connected between V_{SS} and V_{OUT}; even in shutdown. This means that the output resistance will be 350 kΩ (typ.), with a path for output signals to appear at the input. The supply current at V_{SS} includes the current through the load resistor and ladder resistors; it also includes current from the $\overline{CS}$ pin to V_{SS}. When $\overline{CS}$ is low, the amplifier is enabled. If $\overline{CS}$ is left floating, the amplifier may not operate properly.

Figure 1-2 and Figure 2-43 show how the output voltage and supply current response to a $\overline{CS}$ pulse.

4.4 Gain Select (GSEL)

The amplifier can be set to the gains +1 V/V, +10 V/V, and +50 V/V using one input pin (GSEL). At the same time, different compensation capacitors are selected to optimize the bandwidth vs. slew rate trade-off (see Table 4-1). Table 4-2 shows how to change the gain using a GPIO pin on a microcontroller and Table 4-3 shows how to hard wire the gain (i.e., using PCB wiring).

TABLE 4-2: MCU DRIVEN GAIN SELECTION

Gain	MCU Pin's State
+1 V/V	Output PIC's V_{REF} at $V_{DD}/2$
	Digital Output High-Z **(Notes 1)**
	Output $V_{DD}/2$ PWM signal **(Notes 2)**
+10 V/V	Digital Output driven Low
+50 V/V	Digital Output driven High

Note 1: See **Section 4.8.1 "Driving the Gain Select Pin with a Microcontroller GPIO Pin"**.

2: See **Section 4.8.2 "Driving the Gain Select Pin with a PWM Signal"**

TABLE 4-3: HARD WIRED GAIN SELECTION

Selected Gain	Possible GSEL Drivers
+1 V/V	Open Circuit **(Note 1)**
	Low impedance source at $V_{DD}/2$
+10 V/V	Tied to GND (0V)
+50 V/V	Tied to V_{DD}

Note 1: The GSEL pin floats to mid-supply ($V_{DD}/2$); a bypass capacitor may be needed.

4.5 Capacitive Load and Stability

Large capacitive loads can cause stability problems and reduced bandwidth for the MCP6G01/2/3/4 family of SGAs (Figure 2-30 and Figure 2-34). As the load capacitance increases, there is a corresponding increase in frequency response peaking and step response overshoot and ringing. This happens because a large load capacitance decreases the internal amplifier's phase margin and bandwidth.

When driving large capacitive loads with these SGAs (i.e., > 60 pF), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the internal amplifier's stability by making the load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

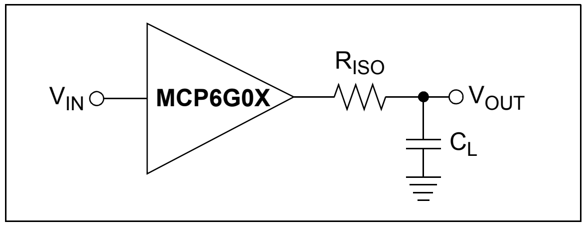


FIGURE 4-5: *SGA Circuit for Large Capacitive Loads.*

Figure 4-6 gives recommended R_{ISO} values for different capacitive loads. After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify R_{ISO}'s value until the response is reasonable at all gains.

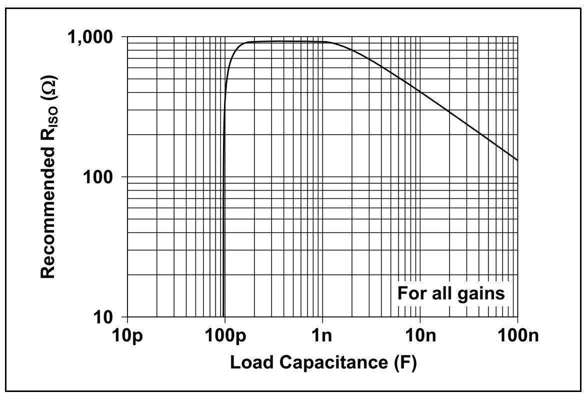


FIGURE 4-6: *Recommended R_{ISO}.*

4.6 Layout Considerations

Good PC board layout techniques will help achieve the performance shown in **Section 1.0 "Electrical Characteristics"** and **Section 2.0 "Typical Performance Curves"**. It will also help minimize Electromagnetic Compatibility (EMC) issues.

Because the MCP6G01/2/3/4 SGAs' frequency response reaches unity gain at 10 MHz when G = 50, it is important to use good PCB layout techniques. Any parasitic coupling at high frequency might cause undesired peaking. Filtering high frequency signals (i.e., fast edge rates) can help.

4.6.1 COMPONENT PLACEMENT

Separate different circuit functions: digital from analog, low speed from high speed, and low power from high power. This will reduce crosstalk.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

4.6.2 SUPPLY BYPASS

Use a local bypass capacitor (0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin for good, high frequency performance. It must connect directly to ground.

Use a bulk bypass capacitor (i.e., 1.0 µF to 10 µF) within 100 mm of the V_{DD} pin. It needs to connect to ground, and provides large, slow currents. This capacitor may be shared with other nearby analog parts.

Ground plane is important, and power plane(s) can also be of great help. High frequency (e.g., multi-layer ceramic capacitors), surface mount components improve the supply's performance.

4.6.3 INPUT SOURCE IMPEDANCE

The sources driving the inputs of the SGAs need to have reasonably low source impedance at higher frequencies. Figure 4-7 shows how the external source resistance (R_S), SGA package pin capacitance (C_{P1}), and SGA package pin-to-pin capacitance (C_{P2}) form a positive feedback voltage divider network. Feedback may cause frequency response peaking and step response overshoot and ringing.

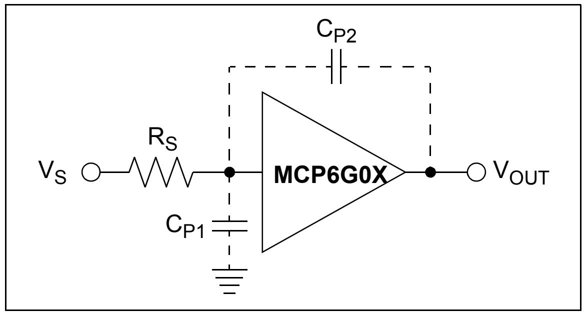


FIGURE 4-7: *Positive Feedback Path.*

Figure 2-10 shows the crosstalk (referred to input) that results when a hostile signal is connected to the other inputs (e.g., V_{INB} through V_{IND}), and the input of interest (e.g., V_{INA}) has R_S connected to GND. A gain of +50 was chosen for this plot because it demonstrates the worst-case behavior. Increasing R_S increases the crosstalk as expected. At a source impedance of 10 MΩ, there is noticeable change in behavior.

Most designs should use a source resistance (R_S) no larger than 10 MΩ. Careful attention to layout parasitics and proper component selection will help minimize this effect. When a source impedance larger than 10 MΩ must be used, place a capacitor in parallel to C_{P1} to reduce the positive feedback. This capacitor needs to be large enough to overcome gain (or crosstalk) peaking, yet small enough to allow a reasonable signal bandwidth.

4.6.4 SIGNAL COUPLING

The input pins of the MCP6G01/2/3/4 family of SGAs are high impedance. This makes them especially susceptible to capacitively coupled noise. Using a ground plane helps reduce this problem.

When noise is capacitively coupled, the ground plane provides additional shunt capacitance to ground. When noise is magnetically coupled, the ground plane reduces the mutual inductance between traces. Increasing the separation between traces makes a significant difference.

Changing the direction of one of the traces can also reduce magnetic coupling. It may help to locate guard traces next to the victim trace. They should be on both sides of, and as close as possible to, the victim trace. Connect the guard traces to the ground plane at both ends. Also connect long guard traces to the ground plane in the middle.

4.7 Unused Amplifiers

An unused amplifier in a quad package (MCP6G04) should be configured as shown in Figure 4-8. This circuit prevents the output from toggling and causing crosstalk. Because the V_{IN} pin looks like an open circuit, the GSEL voltage is automatically set at $V_{DD}/2$, and the gain is 1 V/V. The output pin provides a buffered $V_{DD}/2$ voltage and minimizes the supply current draw of the unused amplifier.

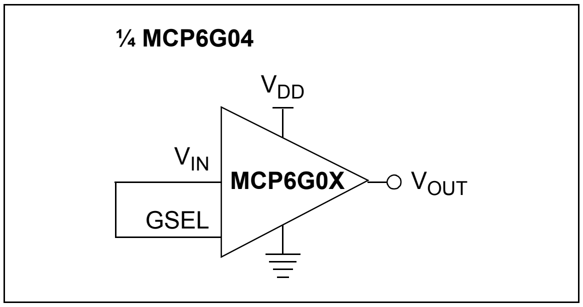


FIGURE 4-8: *Unused Amplifiers.*

4.8 Typical Applications

4.8.1 DRIVING THE GAIN SELECT PIN WITH A MICROCONTROLLER GPIO PIN

The circuit in Figure 4-9 uses a microcontroller GPIO pin to drive the Gain Select input (GSEL). Setting the GPIO pin to logic low, high-Z or logic high gives a GSEL voltage of 0V, $V_{DD}/2$ or V_{DD}, respectively (G = 10, 1 or 50).

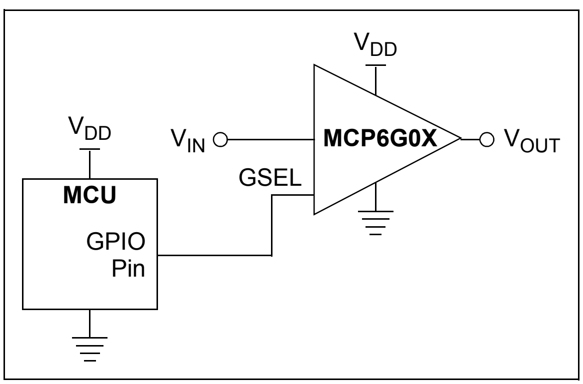


FIGURE 4-9: *Driving the GSEL Pin.*

The microcontroller's GPIO pin cannot produce a leakage current of more than ±1 µA for this circuit to function properly. In noisy environments, a capacitor may need to be added to the GPIO pin.

4.8.2 DRIVING THE GAIN SELECT PIN WITH A PWM SIGNAL

The circuit in Figure 4-10 uses a PWM output on a PIC microcontroller (100 kHz clock rate) to drive the Gain Select input (GSEL). Setting the PWM duty cycle to 0%, 50% or 100% gives a GSEL voltage of 0V, $V_{DD}/2$ or V_{DD}, respectively (G = 10, 1 or 50).

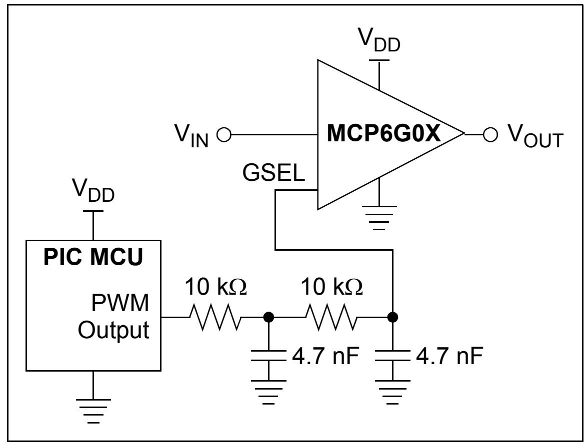


FIGURE 4-10: *Driving the GSEL Pin.*

The PWM clock rate needs to be fast so it is easily filtered and does not interfere with the desired signal, and it needs to be slow enough for good accuracy and low crosstalk. This filter reduces the ripple at the GSEL pin to about 7 mV_{P-P} at V_{DD} = 5.0V. The 10% settling time is about 200 µs; the filter limits how quickly the gain can be changed. Scale the resistors and/or capacitors for other clock rates, or for different ripple.

4.8.3 GAIN RANGING

Figure 4-11 shows a circuit that measures the current I_X. The circuit's performance benefits from changing the gain on the SGA. Just as a hand-held multimeter uses different measurement ranges to obtain the best results, this circuit makes it easy to set a high gain for small signals and a low gain for large signals. As a result, the required dynamic range at the SGA's output is less than at its input (by up to 34 dB).

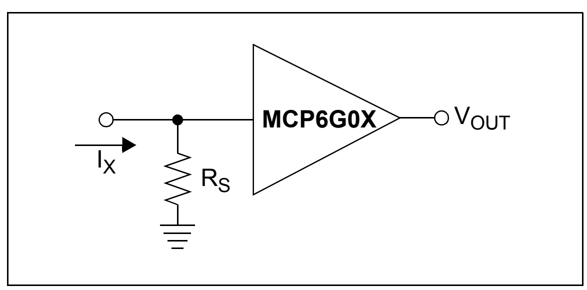


FIGURE 4-11: *Wide Dynamic Range Current Measurement Circuit.*

4.8.4 SHIFTED GAIN RANGE SGA

Figure 4-12 shows a circuit using a MCP6271 at a gain of +10 in front of a MCP6G01. This shifts the overall gain range to +10 V/V to +500 V/V (from +1 V/V to +50 V/V).

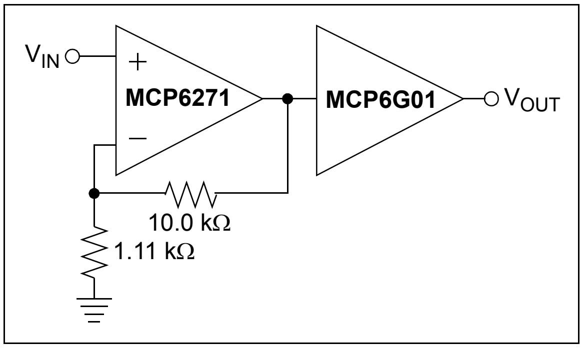


FIGURE 4-12: *SGA with Higher Gain Range.*

It is also easy to shift the gain range to lower gains (see Figure 4-13). The MCP6001 acts as a unity gain buffer, and the resistive voltage divider shifts the gain range down to +0.1 V/V to +5.0 V/V (from +1 V/V to +50 V/V).

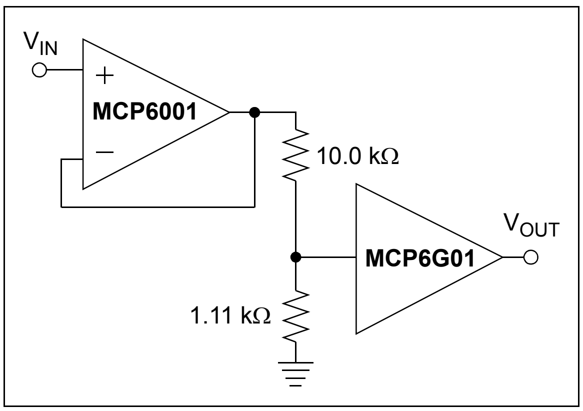


FIGURE 4-13: *SGA with Lower Gain Range.*

4.8.5 ADC DRIVER

This family of SGAs is well suited for driving Analog-to-Digital Converters (ADC). The gains (1, 10, and 50) effectively increase the ADC's input resolution by a factor of as large as 50 (i.e., by 5.6 bits). This works well for applications needing relative accuracy more than absolute accuracy (e.g., power monitoring); see Figure 4-14.

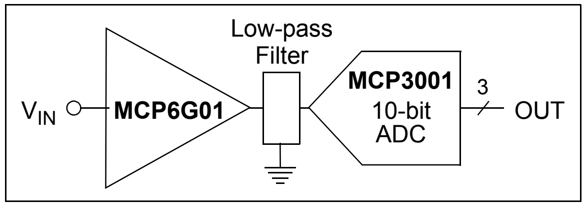


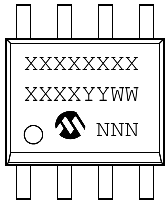
FIGURE 4-14: *SGA as an ADC Driver.*

The low-pass filter in the block diagram reduces the integrated noise at the MCP6G01's output and serves as an anti-aliasing filter. This filter may be designed using Microchip's FilterLab® software, available at www.microchip.com.

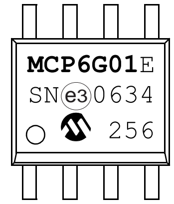
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

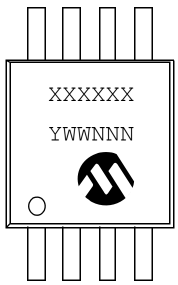
8-Lead SOIC (150 mil) (**MCP6G01**, **MCP6G02, MCP6G03**)



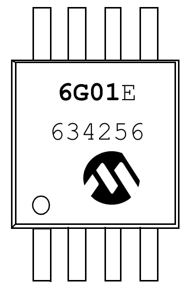
Example:



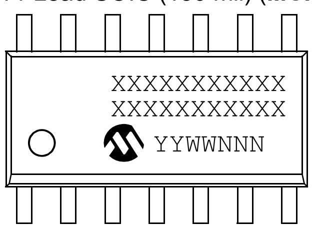
8-Lead MSOP (**MCP6G01**, **MCP6G02, MCP6G03**)



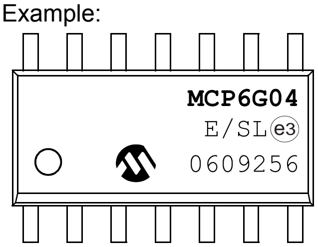
Example:



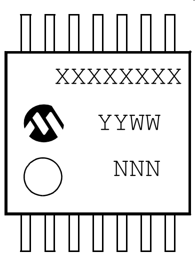
14-Lead SOIC (150 mil) (**MCP6S24**)



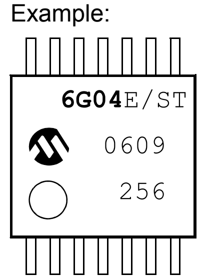
Example:



14-Lead TSSOP (4.4mm) (**MCP6S24**)



Example:

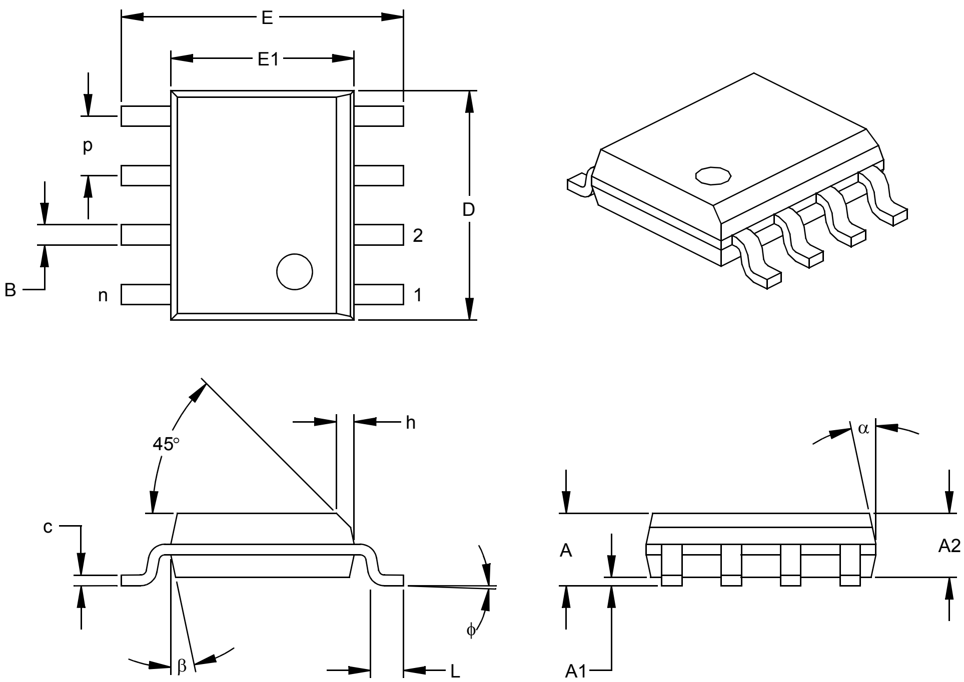


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



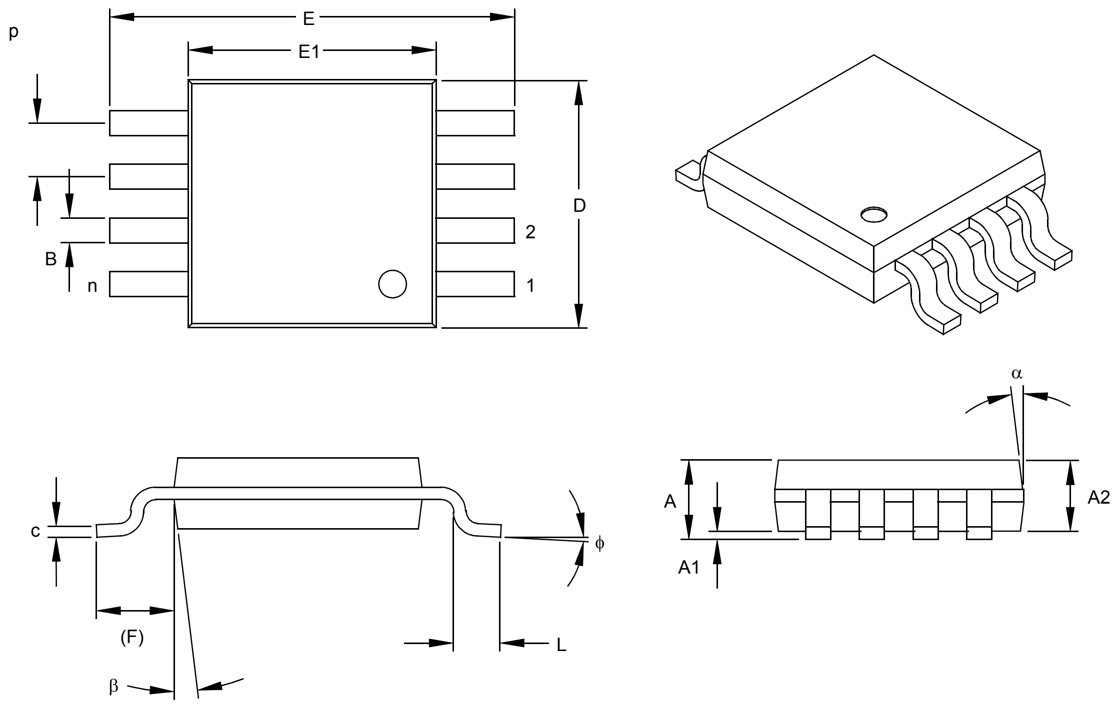
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

*Controlling Parameter
§ Significant Characteristic

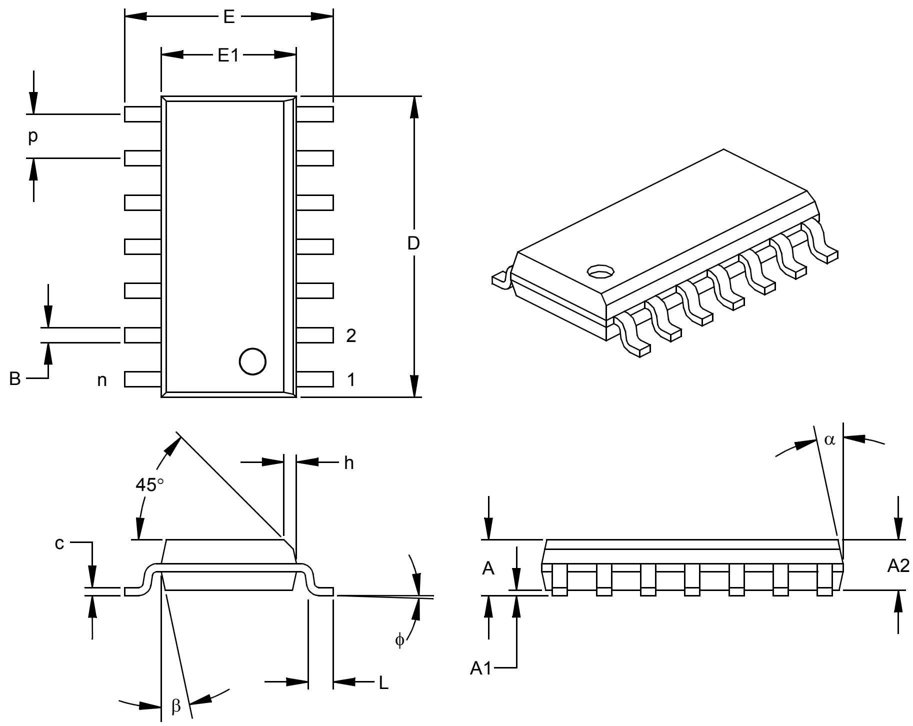
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



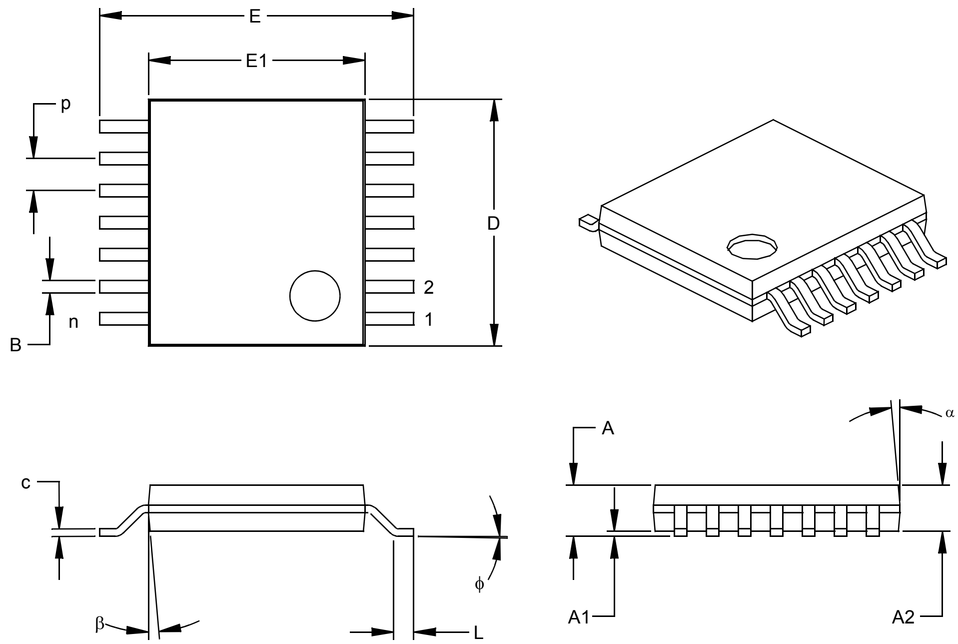
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device:	MCP6G01:	Single SGA
	MCP6G01T:	Single SGA (Tape and Reel for MSOP and SOIC)
	MCP6G02:	Dual SGA
	MCP6G02T:	Dual SGA (Tape and Reel for MSOP and SOIC)
	MCP6G03:	Single SGA
	MCP6G03T:	Single SGA (Tape and Reel for MSOP and SOIC)
	MCP6G04:	Quad SGA
	MCP6G04T:	Quad SGA (Tape and Reel for SOIC and TSSOP)
Temperature Range:	E	= -40°C to +125°C
Package:	MS	= Plastic MSOP, 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead (MCP6G04)
	ST	= Plastic TSSOP (4.4mm Body), 14-lead (MCP6G04)

Examples:

a) MCP6G01-E/MS: Extended Temperature, 8LD MSOP.
b) MCP6G01T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC.

a) MCP6G02-E/MS: Extended Temperature, 8LD MSOP.
b) MCP6G02T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC.

a) MCP6G03-E/MS: Extended Temperature, 8LD MSOP.
b) MCP6G03T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC.
c) MCP6G03-E/SN: Extended Temperature, 8LD SOIC.

a) MCP6G04T-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC.
b) MCP6G04T-E/ST: Tape and Reel, Extended Temperature, 14LD TSSOP.
c) MCP6G04-E/ST: Extended Temperature, 14LD TSSOP.

NOTES:

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